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Name HIEPT NGUYEN
AU 2187 Examiner # 70492
Room # 2A65 Phone 24197
Serial # 09/559,835

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Litigation Searches for the Patent No. 5,765,020.

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Litigation
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1 of 1 DOCUMENT

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5765020

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June 9, 1998

Method of transferring data by transmitting lower order and upper order memory address bits in separate words with respective op codes and start information

REISSUE: Reissue Application filed Apr. 26, 2000 (O.G. Jun. 13, 2000) Ex. Gp.: 2756; Re. S.N. 09/559,835, (O.G. June 13, 2000)

INVENTOR: Barth, Richard Maurice, Palo Alto, CA; Griffin, Matthew Murdy, Mountain View, CA; Ware, Frederick Abbott, Los Altos, CA; Horowitz, Mark Alan, Palo Alto, CA

APPL-NO: 784464 (08)

FILED-DATE: January 16, 1997

GRANTED-DATE: June 9, 1998

ASSIGNEE-AT-ISSUE: Rambus, Inc., Mountain View, CA

ENGLISH-ABST:

A high speed bus system in which at least one master device, such as a processor and at least one DRAM slave device are coupled to the bus. An innovative packet format and device interface which utilizes a plurality of time and space saving features in order to decrease the die size of the device receiver and decrease the overall latency on the bus is provided. In the preferred embodiment the request packet is transmitted on ten multiplexed transmission lines, identified as BusCtl and BusData [8:0]. The packet is transmitted over six sequential bus cycles, wherein during each bus cycle, a different portion of the packet is transmitted. The lower order address bits are moved ahead of the higher order address bits of the memory request. This enables the receiving device to process the memory request faster as the locality of the memory reference with respect to previous references can be immediately determined and page mode accesses on the DRAM can be initiated as quickly as possible. The type of memory access is arranged over a plurality of clock cycles, placing the more critical bits first. The count of blocks of data requested is arranged to minimize the number of bit positions in the packet used and therefore the number of transmission lines of the bus and the number of bus receiver contacts on the receiving device.

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09/559835; Hiep Nguyen; 2187; 70492

?us5765020/pn

** SS 1: Results 1

Search statement 2

?prt full nonstop legalall

1/1 PLUSPAT - (C) QUESTEL-ORBIT- image

PN - US5765020 A 19980609 [US5765020]

TI - (A) Method of transferring data by transmitting lower order and upper order memory address bits in separate words with respective op codes and start information

PA - (A) RAMBUS INC (US)

PA0 - Rambus, Inc., Mountain View CA [US]

IN - (A) BARTH RICHARD MAURICE (US); GRIFFIN MATTHEW MURDY (US); WARE FREDERICK ABBOTT (US); HOROWITZ MARK ALAN (US)

AP - US78446497 19970116 [1997US-0784464]

FD - Cont. of US667293 19960619 [1996US-0667293] (Abandoned)

- Cont. of US484917 19950607 [1995US-0484917] (Abandoned)

- Divsn of US381015 19950130 [1995US-0381015] (Abandoned)

- Cont. of US848421 19920306 [1992US-0848421] (Abandoned)

PR - US78446497 19970116 [1997US-0784464]

- US66729396 19960619 [1996US-0667293]

- US48491795 19950607 [1995US-0484917]

- US38101595 19950130 [1995US-0381015]

- US84842192 19920306 [1992US-0848421]

IC - (A) G06F-013/00

EC - G06F-013/16A2

PCL - ORIGINAL (O) : 710003000; CROSS-REFERENCE (X) : 340825200 340825520
710004000 710030000

DT - Basic

CT - US4247817; US4481625; US4519034; US4523274; US4539677; US4630264;
US4658250; US4701909; US4751701; US4785394; US4785396; US4809264;
US4811202; US4845663; US4860198; US4912627; US4929940; US4959829;
US5012467; US5048009; US5063612; US5124982; US5272700; US5301303;
US5311172; US5319755; US5339307; US5383185; US5408129; WO9102590
- Martin, J. "Local Area Networks: Architectures and Implementations",
pp. 33, 84-88, USA, Prentice-Hall, (1989).

Martin, J. "Local Area Networks: Architectures and Implementations",
pp. 87, 223-224, USA, Prentice-Hall, (1989).

Gumm, Steve L. and Carl T. Dreher, "Unraveling the Intricacies of
Dynamic RAM's", pp. 155-165 Electronic Design News, (Mar. 30, 1989).

STG - (A) United States patent

AB - A high speed bus system in which at least one master device, such as a
processor and at least one DRAM slave device are coupled to the bus.
An innovative packet format and device interface which utilizes a
plurality of time and space saving features in order to decrease the
die size of the device receiver and decrease the overall latency on
the bus is provided. In the preferred embodiment the request packet is
transmitted on ten multiplexed transmission lines, identified as
BusCtl and BusData [8:0]. The packet is transmitted over six
sequential bus cycles, wherein during each bus cycle, a different
portion of the packet is transmitted. The lower order address bits are
moved ahead of the higher order address bits of the memory request.
This enables the receiving device to process the memory request faster
as the locality of the memory reference with respect to previous
references can be immediately determined and page mode accesses on the
DRAM can be initiated as quickly as possible. The type of memory
access is arranged over a plurality of clock cycles, placing the more

09/559835; Hiep Nguyen; 2187; 70492

critical bits first. The count of blocks of data requested is arranged to minimize the number of bit positions in the packet used and therefore the number of transmission lines of the bus and the number of bus receiver contacts on the receiving device.

1/1 LGST - (C) EPO

PN - US5765020 A 19980609 [US5765020]

AP - US78446497 19970116 [1997US-0784464]

ACT - 20000613 US/RF-A

REISSUE APPLICATION FILED

EFFECTIVE DATE: 20000426

UP - 2003-22

1/1 CRXX - (C) CLAIMS/RRX

PN - 5,765,020 A 19980609 [US5765020]

PA - Rambus Inc

ACT - 20000426 REISSUE REQUESTED

Issue Date of O.G.: 20000613

Reissue Request Number: 09/559835

Examination Group responsible for Reissue process: 2756

Search statement 2

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